REMARKS

Claims 1, 2, and 4-25 are now pending in the application. Applicant respectfully informs the Examiner that the outstanding Office Action contained no indication whether the Office Action was Final or non-Final. Applicant has treated the Office Action as non-Final and proceeded to amend the claims in order to expedite prosecution of the application and respectfully asserts that the claimed invention is in condition for allowance. As such, the Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

REJECTION UNDER 35 U.S.C. § 112

The Examiner has objected to the Amendment filed December 2, 2002, under 35 U.S.C. § 112, first paragraph, because it introduces new matter. This rejection is respectfully traversed.

The Examiner alleges that that the claimed "vacant spaces" are not supported by the specification as filed. Applicant respectfully asserts, however, that one skilled in the art would readily appreciate and acknowledge that, in the specification and drawings as filed, the "spaces" are "vacant". More particularly, on page 19 of the application, a method of forming spaces in the bonding layer is described.

"These spaces are formed in the ACF when, in the heating and pressurizing processing, the viscosity of the adhesive rapidly decreases at the initial-process heating (process for approximately 0.1 to 0.5 seconds) so that a portion of the bonding layer flows out toward the exterior of the semiconductor device."

In other words, referring to Figure 2 for example, as the ACF 32 is heated and compressed, the ACF flows outward from the IC 7. This outward flow of the ACF 32 leaves the spaces 33 behind. These spaces are devoid of any material, and are thus, "vacant".

Moreover, Applicant respectfully points the Examiner to MPEP 2163(I)(B) where it states, "While there is no *in haec verba* requirement, newly added claim limitations must be supported in the specification through express, implicit, or inherent disclosure. *In re Oda*, 443 F.2d 1200, 170 USPQ 268 (CCPA 1971) (emphasis added). The claimed invention is directed to a semiconductor device connecting structure for connecting a semiconductor device onto a substrate. The claimed connecting structure utilizes a bonding layer which includes a bonding material for adhering the semiconductor device onto the substrate and a plurality of spaces formed within the bonding material for absorbing deformation of either the semiconductor or the substrate when these elements are subjected to heat and pressure. As stated above, these spaces are formed when the bonding layer is heated, compressed, and caused to flow outward from the semiconductor. As the bonding layer flows outward, one skilled in the art would understand that there is no material present to take its place, and therefore, a vacant space is left behind. As such, Applicant respectfully asserts that the claimed

vacant space is implicitly supported by the disclosure of the invention enumerated by the specification and drawings as originally filed. Accordingly, Applicant respectfully requests that the new matter rejection be reconsidered and withdrawn.

REJECTION UNDER 35 U.S.C. § 102

Claims 1, 8, 18, 24 and 25 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Sato (JP 01-264230). This rejection is respectfully traversed.

Claims 1, 8, 18, 24, and 25 have been amended to call for the vacant spaces to span from the semiconductor device to the substrate. This amendment is fully supported by the application as filed, and can be seen for example, in Figure 1, where the vacant spaces 33 span from the semiconductor device 7 to the substrate 13. Sato does not teach such a structure. Referring to Figure 1 of Sato, it can be seen that the spaces 5 do not span from the semiconductor device 2 to the substrate 4, but are merely minute spaces dispersed throughout the adhesive material. As Sato does not disclose vacant spaces that span from the semiconductor device to the substrate, the claimed invention is not anticipated.

Moreover, Applicant respectfully asserts that Sato contains no teaching, suggestion, or motivation to utilize vacant spaces that span from semiconductor device to the substrate. As stated above, Sato teaches the use of many minute or small spaces. If there is no teaching, suggestion, or motivation, it also would not have been obvious to utilize vacant spaces that span from the semiconductor to the substrate.

Claim 9 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Takeshi (EP 051071). This rejection is respectfully traversed.

The semiconductor connecting method of claim 9 has also been amended to call for the vacant spaces to span from said semiconductor device to said substrate. Moreover, claim 9 has been amended to call for absorbing deformation of the semiconductor device or the substrate with the plurality of vacant spaces. Takeshi does not anticipate such a method. More particularly, Takeshi does not disclose vacant spaces that span from the semiconductor device to the substrate, nor does Takeshi disclose absorbing deformation of the semiconductor device or the substrate with the plurality of spaces. Takeshi, rather, discloses a chip device bonding machine in which bubbles can be effectively prevented from remaining in an adhesive. Takeshi, therefore, in addition to not anticipating the claimed method, also teaches away from the claimed method. As Takeshi teaches away from the claimed method, it also would not have bee obvious to utilize the teachings contained in Takeshi to arrive at the claimed method. Accordingly, reconsideration and withdrawal of this rejection is respectfully requested.

REJECTION UNDER 35 U.S.C. § 103

Claims 2-7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sato as applied to claim 1 and further in view of Andrews (U.S. Pat. No. 5,352,926) and Muramatsu (U.S. Pat. No. 5,893,623). This rejection is respectfully traversed.

Claim 3 was cancelled in the prior Amendment filed in response to the previous Office Action. Claims 2 and 4-7 are dependent on independent claim 1. Applicant respectfully asserts that these claims are not obvious for at least the same reasons as claim 1. More specifically, as stated above, Sato contains no teaching, suggestion, or motivation to utilize vacant spaces that span from the semiconductor device to the substrate. As such, it would not have been obvious.

Claims 11-17 and 19-23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the applicant's admitted prior art in view of Sato and Andrews. This rejection is respectfully traversed.

Claims 11, 17, 19, 20, 22, and 23 have been amended to call for the vacant spaces to span from the semiconductor device to the substrate. As stated in the rejection under 35 U.S.C. § 102(b), Sato does not anticipate such a structure, nor does Sato contain any teaching, suggestion, or motivation. As such, the claimed vacant spaces that span from the semiconductor device to the substrate are not obvious. Accordingly, independent claims 11, 17, 19, 20, 22, and 23, are also not obvious for at least the same reasons.

Dependent claims 12-16 and 21 are also not obvious for at least the same reasons as their independent base claim. It should be noted, however, that the Examiner alleges that dependent claim 21, which calls for a region occupied by the bonding layer to be larger than the mounting area, is obvious in view of routine experimentation or optimization absent a showing of an unobvious purpose, unexpected result, or other criticality. Applicant respectfully asserts that claimed region occupied by the bonding layer is critical for the formation of the claimed vacant spaces. As stated

above, the spaces are formed in the bonding layer when, in the heating and pressurizing processing, the viscosity of the adhesive rapidly decreases at the initial-process heating so that a portion of the bonding layer flows out toward the exterior of the semiconductor device. When the bonding layer flows outward, the vacant spaces are left behind. As such, Applicant respectfully asserts that the dimensions claimed in claim 21 are not obvious in view of the admitted prior art, Sato, Andrews, or any combination thereof.

Claims 10 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Sato as applied to claim 9 and in view of Muramatsu. This rejection is respectfully traversed.

The Examiner rejected claim 10 in view of Sato as applied to claim 9. Claim 9, however, was rejected as being anticipated by Takeshi. Applicant, therefore, has proceeded to address the rejection of claim 10 to also be in view of Takeshi taken further in view of Muramatsu. Applicant respectfully asserts that claim 10, which is dependent on independent claim 9, is not obvious for at least the same reasons as its independent base claim.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance. Thus, prompt

and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

Dated: May 8, 2003

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